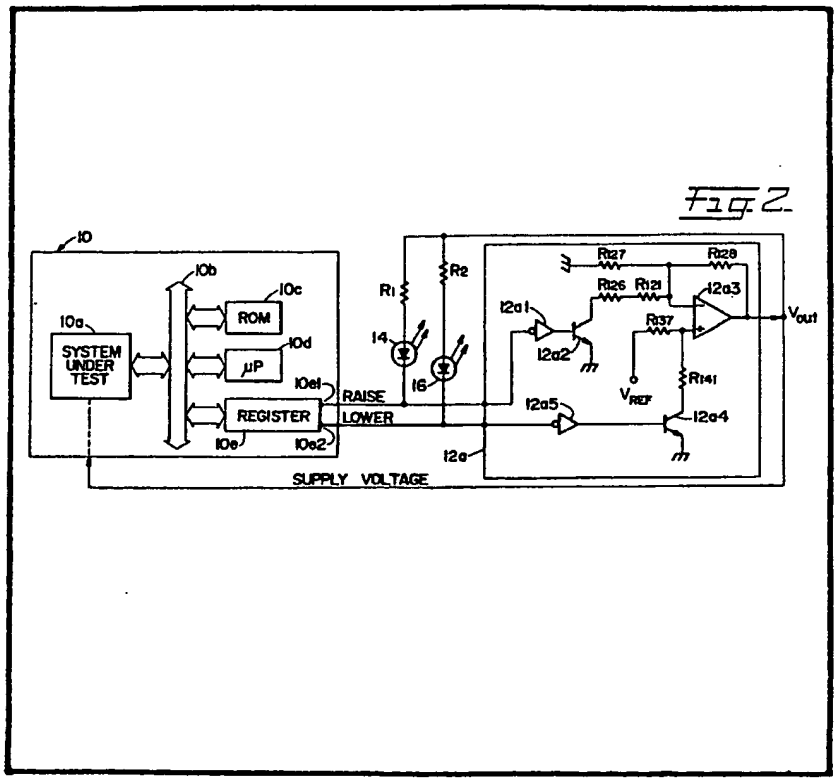
(12) UK Patent Application (19) GB (11) 2 125 973 A

(21) Application No 8319574
(22) Date of filing 20 Jul 1983
(30) Priority data
(31) 410216
(32) 23 Aug 1982
(33) United States of America (US)
(43) Application published 14 Mar 1984
(51) INT CL³ G01R 31/30
(52) Domestic classification G1U C20
(56) Documents cited GB 1255441 WO A 8200896
(58) Field of search G1U
(71) Applicant Tektronix Inc., (USA-Oregon), 4900 S. W. Griffith Drive, P.O. Box 500, Beaverton, Oregon 97077, United States of America
(72) Inventor Keith Wayne Parker
(74) Agent and/or address for service Potts Kerr & Co., 15, Hamilton Square, Birkenhead, Merseyside, L41 6BR

(54) Self-test method and apparatus

(57) A self-test system is disclosed wherein a microprocessor controlled system 10 under test, including a ROM 10*c* and a microprocessor 10*d*, may generate a raise-to-maximum signal. In response to this raise-to-maximum signal, a power supply generates a supply voltage having a magnitude equivalent to the maximum rated voltage of the power supply. A self-test program encoded in the ROM 10*c* directs the microprocessor 10*d* to interrogate the components of the system under test 10*a* when energized by the maximum rated supply voltage. The microprocessor controlled system under test 10 then generates a lower-to-minimum signal. In response to this lower-to-minimum signal, the power supply generates a supply voltage having a magnitude equivalent to the minimum rated voltage of the power supply. The microprocessor 10*d*, under the instructions of the self-test program, interrogates the components of the system under test 10*a* when energized by the minimum rated supply voltage. When the raise-to-maximum signal and the lower-to-minimum signals are not generated, the power supply develops a nominal power supply voltage for energizing the components of the system under test. The components of the system under test are interrogated when energized by the nominal power supply voltage. Since the components of the system under test are energized by a supply voltage having a magnitude ranging from a minimum to a maximum rated power supply voltage while being interrogated by the microprocessor during the self-test mode, all of the defective or potentially defective components of the system under test will fail during the performance of the self-test interrogation. Replacement thereof will ensure that the system will operate more efficiently and more reliably.



GB 2 125 973 A

The drawings originally filed were informal and the print here reproduced is taken from a later filed formal copy.

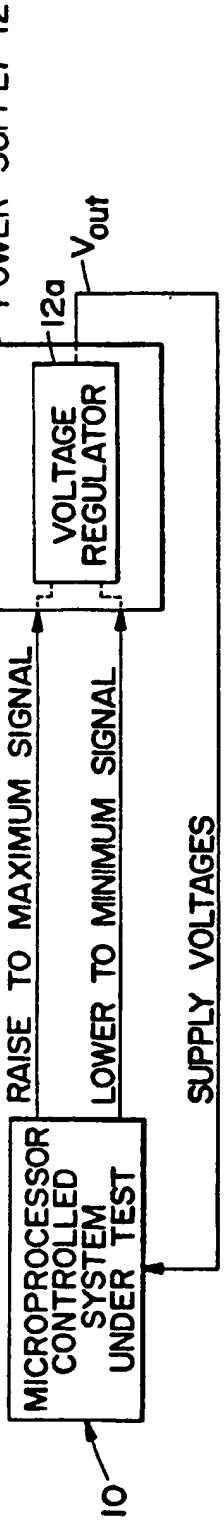
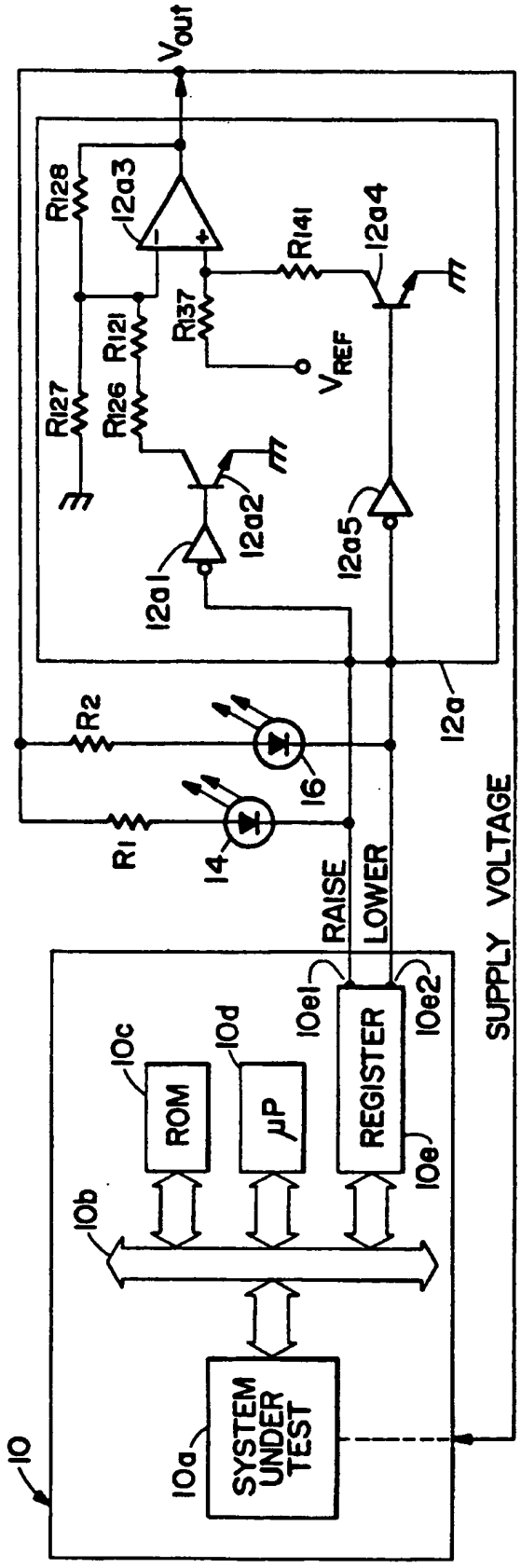

POWER SUPPLY 12
12a
V_{out}
VOLTAGE REGULATOR
RAISE TO MAXIMUM SIGNAL
LOWER TO MINIMUM SIGNAL
SUPPLY VOLTAGES
MICROPROCESSOR CONTROLLED SYSTEM UNDER TEST
10

FIG 1

FIG 2


V_{out}
R128
12a3
R141
12a4
R137
R121
R127
R126
V_{REF}
12a2
12a1
12a5
12a
R2
16
R1
14
RAISE
LOWER
SUPPLY VOLTAGE
10c
ROM
10d
μP
10e1
REGISTER
10e2
10e
10b
10a
SYSTEM UNDER TEST
10

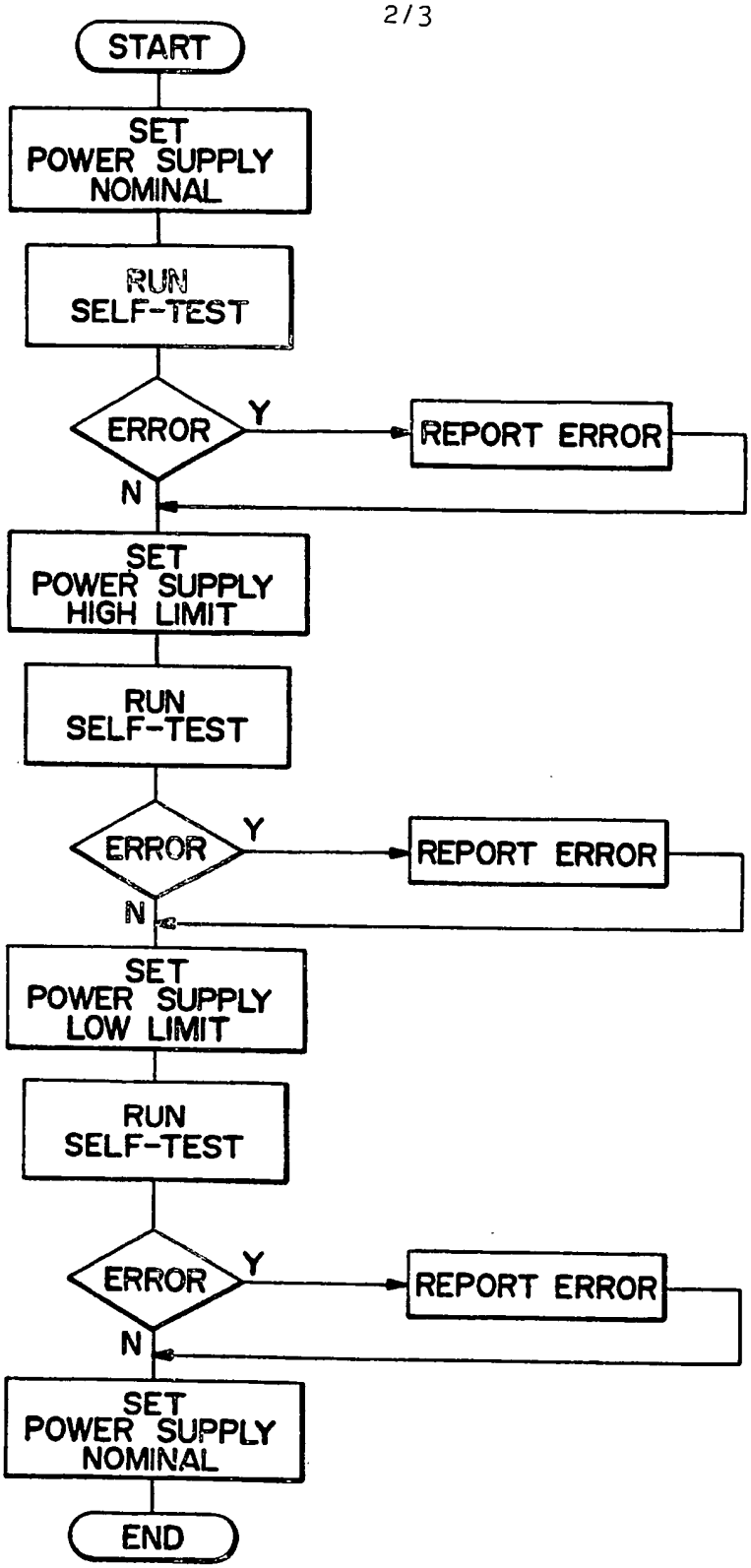
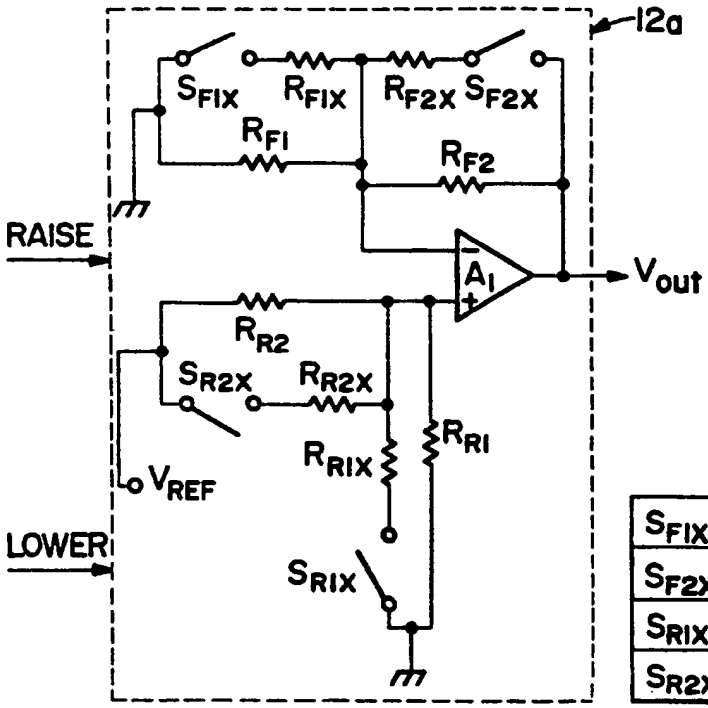
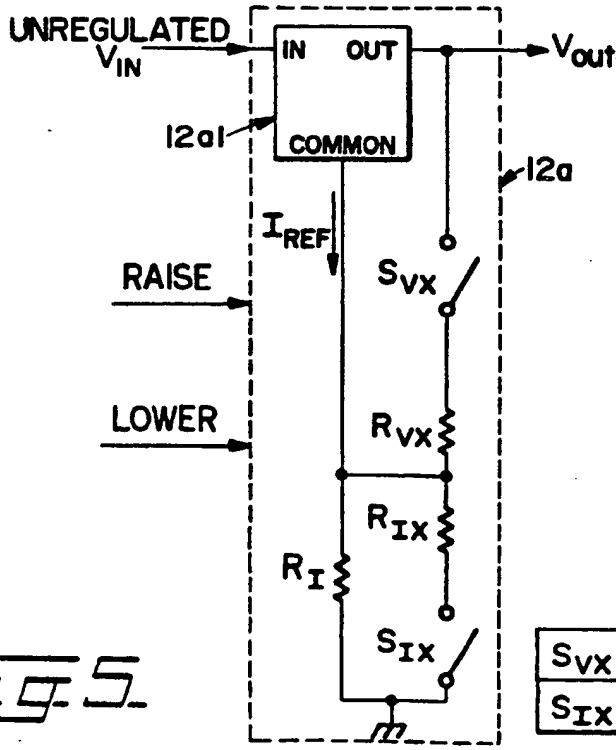

START
SET POWER SUPPLY NOMINAL
RUN SELF-TEST
ERROR
Y
REPORT ERROR
N
SET POWER SUPPLY HIGH LIMIT
RUN SELF-TEST
ERROR
Y
REPORT ERROR
N
SET POWER SUPPLY LOW LIMIT
RUN SELF-TEST
ERROR
Y
REPORT ERROR
N
SET POWER SUPPLY NOMINAL
END

Fig. 3.



	NORMALLY OPEN	NORMALLY CLOSED
S_{F1X}	RAISE	LOWER
S_{F2X}	LOWER	RAISE
S_{RIX}	LOWER	RAISE
S_{R2X}	RAISE	LOWER

Fig. 4.



	NORMALLY OPEN	NORMALLY CLOSED
S_{VX}	RAISE	LOWER
S_{IX}	LOWER	RAISE

Fig. 5.

SPECIFICATION

Self-test method and apparatus

Background of the invention

Field of the invention

The present invention relates to a method and apparatus for testing a system when said system is energized by a wide range of supply voltages in addition to a nominal voltage.

Description of the prior art

A self-test system in an electronic apparatus is utilized for interrogating the circuits of said apparatus during a self-test mode when energized by a nominal voltage from a power supply and analyzing the response received from said circuits in response to the interrogation. An improper response indicates that a failure has occurred within the circuits of said apparatus.

However, self-test systems of the prior art interrogated the circuits during the self-test mode only when the circuits were energized by the nominal voltage from the power supply. Since the circuits were not interrogated, during the self-test mode, when energized by other voltages from the power supply, which differ, in magnitude, from the nominal voltage, some of the components disposed within the circuits failed during a normal operating mode when energized by said other voltages.

Summary of the invention

It is therefore a primary object of the present invention to provide a self-test system for an electronic apparatus which interrogates the circuits disposed within said apparatus, during the self-test mode, when energized by the nominal voltage and by said other voltages ranging in magnitude from a maximum rated magnitude to a minimum rated magnitude.

It is another object of the present invention to provide a first visual indication of the operation of said self-test system in said self-test mode, said first visual indication indicating that said circuits of said apparatus are being interrogated when energized by a voltage having said maximum rated magnitude.

It is still another object of the present invention to provide a second visual indication of the operation of said self-test system in said self-test mode, said second visual indication indicating that said circuits of said apparatus are being interrogated when energized by a voltage having said minimum rated magnitude.

These and other objects of the present invention are accomplished by developing a self-test system which includes a microprocessor for performing the interrogation of the circuits and a new self-test program for directing the operation of said microprocessor in performing the self-test interrogation. The program directs the microprocessor to perform the self-test interrogation when the circuits are energized by the nominal voltage. Then, the program directs the microprocessor to perform the self-test interrogation when the circuits are sequentially energized by a voltage having said maximum rated magnitude and by a voltage having said minimum rated magnitude. When the program directs the microprocessor to perform the self-test interrogation utilizing the voltage having the maximum rated magnitude, a bit in a register is set. An output signal from the register is developed in response thereto, the output signal energizing a power supply. A voltage regulator in the power supply develops an output signal, the output signal from the voltage regulator being raised from a level corresponding to the nominal voltage to a level corresponding to said maximum rated magnitude in response to the output signal from the register. At this point, the microprocessor performs the interrogation of the circuits in said apparatus when energized by the voltage having said maximum rated magnitude. Similarly, when the program directs the microprocessor to perform the self-test interrogation utilizing the voltage having the minimum rated magnitude, another bit in the register is set. Another output signal is developed from the register in response thereto, said another output signal energizing said power supply. The voltage regulator in said power supply develops an output signal, the output signal from the voltage regulator being lowered from the nominal level to a level corresponding to said minimum rated magnitude in response to said another output signal from the register. At this point, the microprocessor performs the interrogation of the circuits when energized by the voltage having said minimum rated magnitude. Since the components of the circuits are tested when energized by a wide range of supply voltages, all of the potentially defective components will be detected. Replacement thereof will ensure a more reliable operation of the circuits of said apparatus.

Further scope of applicability of the present invention will become apparent from the description given hereinafter. However, it should be understood that the details of the description on the specific examples, while indicating preferred embodiments of the invention, are given by way of illustration only, since various changes and modifications within the spirit and scope of the invention will become apparent to those skilled in the art from the detailed description.

Brief description of the drawings

A full understanding of the present invention will be obtained from the detailed description given hereinbelow and the accompanying drawings, which are given by way of illustration only, and thus are not limitative of the present invention, and wherein:

Fig. 1 illustrates a basic system block diagram illustrating the principles of the present invention.

Fig. 2 illustrates a more detailed system block diagram illustrating the principles of the present invention.

Fig. 3 illustrates a flow chart representative of the self-test program encoded in a ROM, one of

the components of the microprocessor controlled system under test shown in Figs. 1 and 2.

Fig. 4 illustrates an alternative embodiment of a voltage regulator, a component of the system block diagrams shown in Figs. 1 and 2.

Fig. 5 illustrates another alternative embodiment of the voltage regulator, a component of the system block diagrams shown in Figs. 1 and 2.

Detailed description of the drawings

Referring to Fig. 1, a basic system block diagram of the present invention is illustrated. A microprocessor controlled system under test 10 includes a system under test, such as in integrated circuit chip, and a microprocessor connected thereto. The microprocessor controlled system under test 10 may be, for example, a single-chip microcomputer, such as an Intel 8748. The microprocessor performs the self-test interrogation of the components of the system under test. The microprocessor interrogates the system under test, during the self-test mode, when the system is energized by the nominal voltage from the power supply. A response is received from the system in response to the interrogation. The response is analyzed. If an improper response is received, associated with one or more of the components of the system under test, the associated components are potentially defective. This represents an error condition, which is so reported.

However, during the normal operating mode, the system may be energized by other voltages from the power supply which differ in magnitude from the nominal voltage. Consequently, the components of the system under test may fail when energized by said other voltages. In order to test the components of the system under test, during the self-test mode, when energized by said other voltages, the microprocessor controlled system under test 10 develops a "raise to maximum" signal and a "lower to minimum" signal. A power supply 12 is connected to the microprocessor controlled system under test 10 and receives the "raise to maximum" signal and the "lower to minimum" signal therefrom. More specifically, a voltage regulator 12A, within the power supply 12 receives the "raise to maximum" signal and the "lower to minimum" signal. When the voltage regulator 12A is energized by the "raise to maximum" signal, a power supply voltage signal is developed therefrom at an output terminal thereof in response thereto representative of the maximum rated voltage of the power supply 12. When the voltage regulator 12A, within the power supply 12, receives the "lower to minimum" signal, another power supply voltage signal is developed therefrom at said output terminal thereof in response thereto representative of the minimum rated voltage of the power supply.

The output terminal of the voltage regulator 12a is connected, in feedback fashion, to the microprocessor controlled system under test 10. When the microprocessor controlled system under test 10 is energized by the power supply voltage signal representative of the maximum rated voltage of the power supply 12, the microprocessor controlled system under test 10, and specifically the microprocessor, performs the self-test interrogation of the system under test, when energized by the power supply voltage signal representative of the maximum rated voltage of the power supply. Further, the microprocessor control system under test 10 performs the self-test interrogation of the system under test when energized by the power supply voltage signal representative of the minimum rated voltage of the power supply.

When the "raise to maximum" signal, and the "lower to minimum" signal is not developed by the microprocessor controlled system under test 10, the voltage regulator 12A within the power supply 12, generates a power supply voltage signal equivalent to the nominal voltage of the power supply. The microprocessor controlled system under test 10 then performs the self-test interrogation of the system under test, when energized by the nominal voltage of the power supply. Consequently, the components of the system under test are tested, when energized by the nominal supply voltage, the maximum rated power supply voltage, and the minimum rated power supply voltage. Therefore, an increased number of the potentially defective components of the system under test will be identified. Their replacement thereof will ensure that the system will operate more reliably during the normal operating mode than would otherwise be true had such a wide-range self-test interrogation not been performed.

Referring to Fig. 2, a more detailed system block diagram of the present invention is illustrated. The microprocessor controlled system test 10 further includes a system under test 10A. The system under test 10A is connected to a system bus 10B. A read-only memory (ROM) 10C is connected to the system bus 10B. A microprocessor (μP) 10D is also connected to the system bus 10B. An Intel 8086 may be used for the microprocessor 10D. A register 10E is connected to the system bus 10B. A first output terminal 10E1 of the register 10E is connected to the voltage regulator 12A. A second output terminal 10E2 of the register 10E is connected to the voltage regulator 12A. The voltage regulator 12A further includes a first inverter 12A1, the input terminal thereof being connected to the first output terminal 10E1 of the register 10E. The output of the inverter 12A1 is connected to the base of a transistor 12A2. The emitter of the transistor is connected to a ground potential. The collector of the transistor 12A2 is connected to a first resistor R126. A second resistor R121 is connected in series with the first resistor R126. The output of the second resistor R121 is connected to a negative input terminal of a comparator 12A3. The negative input terminal of the comparator 12A3 is also connected to the

output terminal of a resistor R127. The input terminal of the resistor R127 is grounded. Further, the negative input terminal of the comparator 12A3 is connected to the input terminal of another resistor R128, the output of said another resistor R128 being connected to the output terminal of the comparator 12A3.

The voltage regulator 12A further includes a second inverter 12A5, the input terminal thereof being connected to the second output terminal 10E2 of the register 10E. The output terminal of the inverter 12A5 is connected to the base of a second transistor 12A4. The emitter of the second transistor 12A4 is connected to a ground potential. The collector of the second transistor 12A4 is connected to the input terminal of a resistor R141. The output terminal of the resistor R141 is connected to the positive input terminal of the comparator 12A3. The positive input terminal of the comparator 12A3 is also connected to the output terminal of a resistor R137. The input terminal of the resistor R137 is connected to a reference voltage source (VREF).

The output terminal of the comparator 12A3 generates the power supply voltage signal from the voltage regulator 12A within the power supply 12 shown in Fig. 1. This output terminal of the comparator 12A3 is connected, in feedback fashion to the system under test 10A, within the microprocessor control system under test 10. The output terminal of the comparator 12A3 is also connected to the first output terminal 10E1 of the register 10E via the series connection of a resistor R1 and a first light emitting diode (LED) 14. Furthermore, the output terminal of the comparator 12A3 is connected to the second output terminal 10E2 of the register 10E via the series connection of a resistor R2 and a second light emitting diode (LED) 16.

Referring to Fig. 3, a flow chart of the self-test program contained within the ROM 10C of the microprocessor controlled system under test 10 is illustrated. In Fig. 3, initially, the program sets the power supply to its nominal limit whereby the nominal power supply voltage is generated. The microprocessor 10D then performs the self-test interrogation of the system under test 10A when energized by the nominal power supply voltage. If an error is detected, the error is so reported. At this point, the self-test program sets the power supply to its high limit whereby the maximum rated power supply voltage is generated. The microprocessor 10D then performs the self-test interrogation of the system under test 10A, when energized by the maximum rated power supply voltage. Again, if an error is detected, the error is so reported. Finally, the self-test program sets the power supply to its low limit whereby the minimum rated power supply voltage is generated. The microprocessor 10D performs the self-test interrogation of the system under test 10A when energized by the minimum rated power supply voltage. If an error is detected, the error is so reported.

The operation of the circuit shown in Fig. 2 of the drawings of the present application will now be described in the paragraphs hereinbelow.

The self-test program encoded in the ROM 10C, within the microprocessor controlled system under test 10, directs the microprocessor 10D to energize the system under test 10A with the nominal power supply voltage from the power supply 12. In response to this direction, the register 10E does not develop an output signal from either the first or the second output terminals, 10E1 or 10E2, thereof. Therefore, the "raise to maximum" signal and the "lower to minimum" signal is not generated. As a result, the power supply 12 develops the nominal power supply voltage for energizing the system under test. The microprocessor, at this point, interrogates the components of the system under test, soliciting responses in response thereto, analyzing the responses to determine if an erroneous response was received.

The self-test program encoded in the ROM 10C then instructs the microprocessor 10D to generate an output signal via the system bus 10B for energizing the register 10E. A bit in the register 10E is changed from "1" to "0". As a result, the "raise to maximum" signal is generated from the register 10E. This "raise to maximum" signal is inverted via the inverter 12A1 such that a high output signal is developed therefrom. The high output signal from the first inverter 12A1 causes the first transistor 12A2 to conduct. When the first transistor 12A2 conducts, the series connected resistors R126 and R121 are connected to ground. This, in turn, causes resistor R127 and the series connected resistors R126 and R121 to be connected in parallel with one another. As a result of the parallel connection of resistor R127 and resistors R126 and R121, the resistance of the lower leg of the feedback loop is reduced. As a consequence of this, the voltage present at the negative input terminal of the comparator 12A3 is reduced. As a result, the output signal present at the output terminal of the comparator 12A3 is increased, in order to compensate for the reduction in the voltage present at the negative input terminal thereof. The output terminal of the comparator 12A3 is connected to the system under test. Since the output voltage of the voltage regulator 12A is increased in response to the generation of the "raise to maximum" signal, an increased power supply voltage (the maximum rated voltage of the power supply) energizes the system under test 10A.

The "raise to maximum" signal, generated from the register 10E, is a low level signal. As a result, the first light-emitting diode 14 conducts. Current flows through the first light-emitting diode 14 via resistor R1, causing light to be emitted therefrom. This represents a visual indication that the self-test system is operating in a self-test mode, and the components of the system are energized by a voltage having said maximum rated magnitude.

While the system under test 10A is energized

by the increased power supply voltage supplied from the voltage regulator 12A, the self-test program in the ROM 10C directs the microprocessor to perform the self-test interrogation, wherein the various components of the system under test will be interrogated in order to solicit responses therefrom in response thereto while energized by the voltage having said maximum rated magnitude. The responses are analyzed to determine if an improper response has been generated from the respective components of the system under test 10A. If an improper response is received, the microprocessor reports the error. This error indicates that some of the respective components of the system are potentially defective.

At this point, the self-test program encoded in the ROM 10C instructs the microprocessor 10D to generate an output signal via the system bus 10B, to change a bit in the register 10E from "1" to "0", such that the "lower to minimum" signal is generated therefrom. This "lower to minimum" signal is applied to the input of the second inverter 12A5, which inverts the signal applied thereto. A high output signal is generated therefrom, the high output signal being applied to the base of the second transistor 12A4. As a result, the second transistor 12A4 conducts. When the transistor 12A4 conducts, resistor R141 is connected to a ground potential. This, effectively, creates a voltage divider network comprising resistors R141 and R137. A voltage reference (VREF) is applied to an input terminal of R137. As a result of this voltage divider network, the voltage applied to the positive input terminal of the comparator 12A3 is reduced in magnitude from

VREF to (R141) (VREF)/-(R141+R137).

As a result of the reduction in the magnitude of the voltage applied to the positive input terminal of the comparator 12A3, the voltage present at the output terminal of the comparator 12A3 is also reduced in magnitude. Again, since the output of the comparator 12A3 is connected to the system under test, a reduced power supply voltage (the minimum rated voltage of the power supply) is applied to the system under test 10A.

At this point, the microprocessor 10D, in accordance with the instructions of the self-test program encoded in the ROM 10C, performs the self-test interrogation once again, wherein the individual components of the system under test are interrogated when energized by the reduced power supply voltage. The response received by the microprocessor 10D, as a result of this interrogation, is analyzed to determine if a proper response has been received. If an improper response has been received, the microprocessor reports the error.

When the "lower to minimum" signal is generated from the register 10E, a low level signal is generated. This low level signal causes the second light-emitting diode 16 to conduct. Current then flows from the output terminal of the comparator 12A3, through the resistor R2, and through the light-emitting diode 16 for generating light in response thereto. This represents a visual indication that the self-test system is operating in a self-test mode, and the components of the system under test are energized by a voltage having said minimum rated magnitude.

Referring to Fig. 4, one alternative embodiment of the voltage regulator 12a, as shown in Figs. 1 and 2, is illustrated. If the raise to maximum signal is received by the voltage regulator 12 as shown in Fig. 4, there are four different methods for raising the output voltage (V_{out}) in response thereto. Four switches are shown in Fig. 4, switches S_{F1X}, S_{F2X}, S_{1X}, S_{R2X}. If switches S_{F1X} and S_{R2X} are normally open, assuming the other switches remain in their open position as shown in Fig. 4, closing either switch S_{F1X} or switch S_{R2X} will raise the output voltage (V_{out}). If switches S_{F2X} and S_{R1X} are normally closed, assuming the other switches remain in their open position as shown in Fig. 4, opening either switch S_{F2X} or switch S_{R1X} will raise the output voltage (V_{out}).

Similarly, there are four different methods for lowering the output voltage (V_{out}) of the voltage regulator 12a shown in Fig. 4 in response to the lower to minimum signal received thereby. If the switches S_{F2X} and S_{R1X} are normally open, assuming the other switches remain in their open position as shown in Fig. 4, closing either switch S_{F2X} or S_{R1X} will lower the output voltage (V_{out}). Similarly, if switches S_{F1X} and S_{R2X} are normally closed, assuming the other switches remain in their open position, as shown in Fig. 4, opening either switch S_{F1X} or switch S_{R2X} will lower the output voltage (V_{out}).

In the above description, it is assumed that the "raise to maximum" signal would close either one of the normally open switches S_{F1X} or S_{R2X}. Alternatively, the raise to maximum signal would open either one of the normally closed switches S_{F2X} or S_{R1X}. Similarly, the lower to minimum signal would close either one of the normally open switches S_{F2X} or S_{R1X}. Alternatively, the lower to minimum signal would open either one of the normally closed switches S_{F1X} or S_{R2X}.

In Fig. 5, another alternative embodiment of the voltage regulator 12a, shown in Figs. 1 and 2, is illustrated. In Fig. 5, two switches are illustrated, switches S_{VX} and S_{IX}. If the raise to maximum signal is received, if normally open switch S_{VX} is closed, assuming that the other switch remains in its open position as shown in Fig. 5, the output voltage (V_{out}) is raised. If the switch S_{IX} is normally closed, and if switch S_{IX} is opened, the output voltage (V_{out}) is raised. If the lower to minimum signal is received, and if the normally open switch S_{IX} is closed, assuming that the other switch remains in its open position as shown in Fig. 5, the output voltage (V_{out}) will be lowered. Similarly, if the switch S_{VX} is normally closed, and if switch S_{VX} is opened, assuming that the other switch remains in its open position as shown in Fig. 5, the output voltage (V_{out}) will be

lowered In Fig. 5, an adjustable three-terminal voltage regulator 12a1 is utilized.

The invention being thus described, it will be obvious that the same may be varied in many ways. Such variations are not to be regarded as a departure from the spirit and scope of the invention and all such modifications as would be obvious to one skilled in the art are intended to be included within the scope of the following claims.

Claims

1. A self-test system, comprising:

first means connected to a system under test for developing a first output signal and a second output signal;

second means connected to said first means and to said system under test and responsive to said first and second output signals from said first means for developing a nominal signal when not energized by said first and said second output signals, said second means developing a maximum signal having a magnitude greater than the magnitude of said nominal signal when energized by said first output signal, said second means developing a minimum signal having a magnitude lower than the magnitude of said nominal signal when energized by said second output signal, said nominal signal, said maximum signal, and said minimum signal energizing said system under test,

said first means interrogating the components of said system under test while energized by said nominal signal,

said first means interrogating the components of said system under test while energized by said maximum signal,

said first means interrogating the components of said system under test while energized by said minimum signal.

2. The self-test system of claim 1 further comprising:

first indication means for providing a first indication that said first output signal is generated from said first means.

3. The self-test system of claim 1 further comprising:

second indication means for providing a second indication that said second output signal is generated from said first means.

4. A method of testing the components of a system under test, comprising the steps of:

energizing the components of said system under test with a nominal voltage;

interrogating said components while energized by said nominal voltage and analyzing a response received as a result of the interrogation;

energizing said components with a maximum voltage having a magnitude greater than the magnitude of said nominal voltage;

repeating the interrogating and analyzing steps while said components are energized by said maximum voltage;

energizing said components with a minimum voltage having a magnitude less than the magnitude of said nominal voltage; and

repeating the interrogating and analyzing steps while said components are energized by said minimum voltage.

5. A self-test system substantially as hereinbefore described with reference to and as illustrated in the accompanying drawings.

6. A method of testing the components of a system under test substantially as hereinbefore described.

Printed for Her Majesty's Stationery Office by the Courier Press, Leamington Spa, 1984. Published by the Patent Office, 25 Southampton Buildings, London, WC2A 1AY, from which copies may be obtained.